Ezekiel Moses Sequeira

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Motivated Electronics and Communication Engineering student with a strong foundation in VLSI design, semiconductor fundamentals, and physical verification. Passionate about DRC/LVS verification, circuit design, and full-custom VLSI flow, with hands-on experience in Cadence Virtuoso and Assura. Possessing strong analytical, problem-solving, and collaboration skills with a commitment to continuous learning and innovation in semiconductor technologies.

Education

National Institute of Technology, Goa, India (Oct '22 - Present)

- **Degree in Bachelor of Technology in Electronics and Communication Engineering** **CGPA: 9.55/10**

Relevant Subjects: Analog Electronics (EC201), Digital Electronics (EC251), Electromagnetic Theory (EC204), Network Theory (EC203), Control System(EC302), VLSI Circuit Design (EC401), Computer Architecture and Organization(EC406), Low Power VLSI Circuit Design (EC424)

- **Minor Degree of Technology in Computer Science Engineering** **CGPA: 9.61/10**

Relevant Subjects: Data Structures and Algorithms (CS250M), Design and Analysis of Algorithm (CS300M), Database Management System(CS350M), Data Science Fundamentals with Python(CS400M)

The Indian School, Kingdom of Bahrain (Apr '20-Apr '22)
Computer Science in Central Board of Secondary Education (CBSE) **GPA: 10/10**

The Indian School, Kingdom of Bahrain (Apr '10-Apr '20)
Science in Central Board of Secondary Education (CBSE) **Grade: 93%**

Work Experience

Research Intern (Onsite)
Indian Institute of Technology (IIT) Madras,India (May '25 – Jul '25)

- Worked under faculty guidance at IIT Madras on a distributed acoustic sensing (DAS) system
- Completed an 8-week research internship focused on analog front-end design and simulation
- Contributed to circuit architecture, biasing schemes, and impedance matching
- Used TINA-TI to analyze parasitics and optimize inter-stage coupling performance
- Gained hands on experience in circuit simulation, performance tuning, and signal integrity optimization in high-frequency analog systems

Project Experience

Rail-to-Rail Comparator Design (Feb '26 – Ongoing)
Technologies: Cadence Virtuoso, Assura

- Designing a CMOS dynamic comparator full input common-mode range.
- Reduced propagation delay by ~100 ps vs. traditional designs.
- Maintained comparable kickback noise and offset voltage.
- Performing pre-layout simulations and corner analysis.

Detection of Chagas Disease using AI on 12-Lead ECG (Jun '25 – Ongoing)
Technologies used: Python, TensorFlow/Keras, NumPy, Pandas, Scikit-learn, Matplotlib

- Designing an AI system to detect Chagas disease from 12-lead ECG signals.

- Implementing scalograms, statistical/HRV features, and Tucker decomposition for dimensionality reduction.
- Ensuring robust model performance with metadata augmentation, SMOTE balancing, and patient-wise evaluation.

Design of 8-bit Arithmetic Logic Unit (ALU) (Sep ’25 – Dec ‘25)
Technologies used: Cadence Virtuoso, Assura

- Designed and implemented an 8-bit ALU from transistor level circuits in 180 nm CMOS technology
- Executed full-custom VLSI flow from schematic capture to post-layout verification, including DRC/LVS checks in Assura and resolving layout-rule violations.
- Integrated arithmetic and logic functional blocks to support 15 distinct operations.
- Developed a novel logic cell (Approved for presentation at NEWCAS 2026) .
- Achieved ~88 μW power reduction and ~200 ps delay improvement over standard CMOS designs.

Distributed Acoustic Sensing (DAS) System,Analog Front-End (May ‘25 – Jul ‘25)
Technologies used: TINA-TI, LT-Spice

- Designed a high-gain, wideband three-stage amplifier for a distributed acoustic sensing (DAS) system
- Optimized for integration with a balanced photodetector (BPD), achieving 108 dB gain and 100 MHz bandwidth
- Mitigated parasitic capacitance and stabilized bias currents using compensation techniques
- Achieved impedance matching between stages within ±5% for consistent signal performance

Design of 8-bit CPU (Jun ‘24-Oct ‘24)
Technologies used: LT-Spice, Logisim-Evolution, Excel VBA

- Designed an 8-bit CPU based on the Von Neumann architecture, inspired by the 8085 microprocessor.
- Designed a custom instruction set and built a compiler in Excel VBA to convert high level code to machine code
- Implemented an ALU capable of performing 7 operations, a hardwired control unit, 4 general-purpose registers.
- Verified the CPU by testing 10+ custom programs, achieving accurate simulation for expected outputs.

Analog Communication & Pulse Electronics Projects (Oct ’23 – May ’24)
Technologies: LTspice

- Designed a low-power AM transmitter operating at 1 MHz (MW band).
- Achieved stable transmission with minimal frequency drift over a 6–8 ft range
- Built a compact EMP generator producing high-voltage pulses.
- Demonstrated disruption of nearby electronics within a 0.1–0.2 m range.
- Validated functionality on basic devices such as calculators.

Additional Skills

- **Programming Languages**: Matlab, Python, C, C++, Verilog HDL,
- **Technical Knowledge:** Analog electronics, Computer Organization, Digital Electronics ,Control Systems,
- **Communication Skills:** English Speaking, Team player,

Achievements and Awards

- **Merit based Selection from 255 students:** Top **11.8%** for **Degree in Computer Science & Engineering**.
- **Certificate of Distinction** for **A1 in all subjects** (12th) among **624 students.**
- **Physics topper** and **Third place in stream** in 12th Science among **624 students.**
- **Recognition** in **The Gulf Daily News, Bahrain newspaper** (23rd July 2022) **for 10 CGPA** in 12th standard.
- **Recognition** in **The Daily Tribune, Bahrain Newspapers** (23rd July 2022) for **12th academic excellence.**
- **Finalist** in the **All India SASTRA-Pratibha Technology Competition, among 100,000 students.**